(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 450 082 A1**

(12) **EUROPEAN PATENT APPLICATION published in accordance with Art. 158(3) EPC**

(21) Application number: 90912955.3

(22) Date of filing: 29.08.90

(86) International application number: PCT/JP90/01091

(87) International publication number: WO 91/03842 (21.03.91 91/07)

(51) Int. Cl.5: H01L 29/784

(30) Priority: 31.08.89 JP 226262/89

(43) Date of publication of application: 09.10.91 Bulletin 91/41

(84) Designated Contracting States: DE FR GB

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(54) **INSULATED GATE BIPOLAR TRANSISTOR.**

(57) An insulated gate bipolar transistor having a reverse conduction function and comprising a semiconductor layer of a first conductivity type on the drain side, a semiconductor layer of a second conductivity type formed thereon to develop conduction modulation upon injection of carriers, a semiconductor layer of the second conductivity type that is formed in the above semiconductor layer of the second conductivity type and electrically connected to the drain electrode to take out the reverse conduction current flowing in a direction opposite to the drain current, and a semiconductor layer of the second conductivity type that is formed in the boundary surface or near the boundary surface of pn junction where the carriers are transferred to effect conduction modulation, and that has a high impurity concentration so as to serve as a path of the reverse conduction current and has a pattern which does not impair the transfer of the carriers. Owing to the above construction, there is incorporated a reverse conduction function having a small operation resistance, and it is allowed to flow a large current in the reverse direction, preventing the on-resistance from increasing and shortening the turn-off time.

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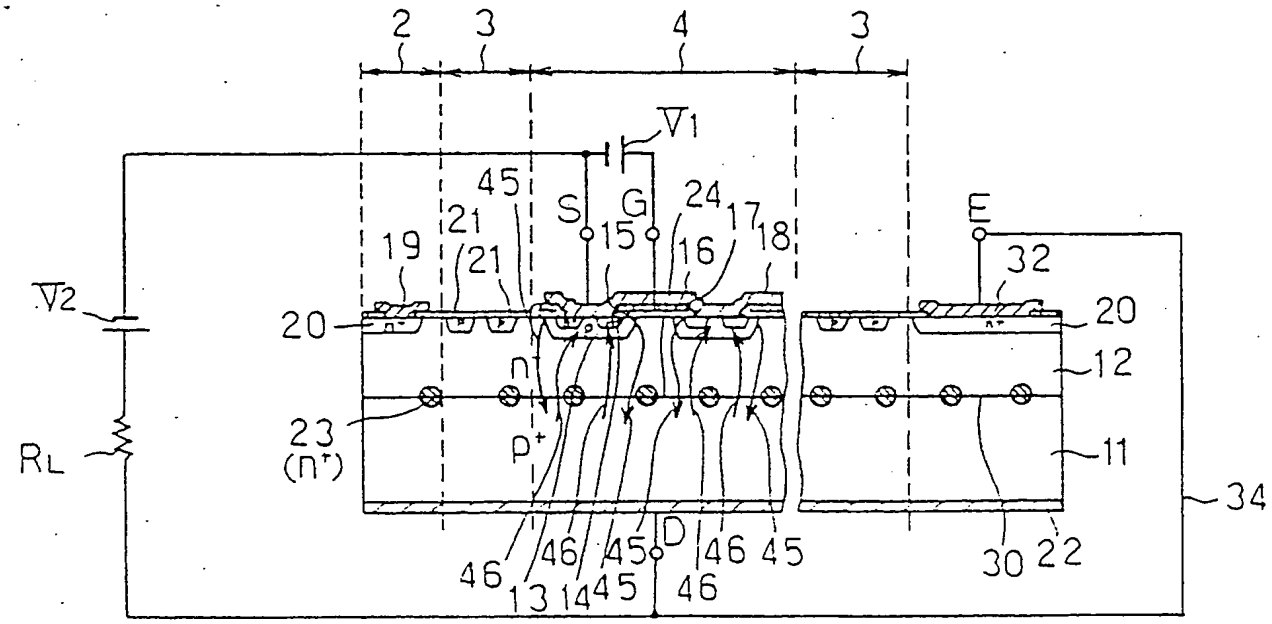
FIG.2



TECHNICAL FIELD

This invention relates to an insulated gate bipolar transistor having a reverse conducting function built therein.

BACKGROUND ART

Recently, attention has been paid to insulated gate bipolar transistors (referred to as IGBT) as shown in Fig. 14 that are usable as power elements for which high withstand voltage and low on-resistance are required.

Since this type of transistor has a p^+ layer on the side of a drain D, a low on-resistance is attained; but, its turn-off time is long as compared with a usual power MOSFET.

Generally, power switching elements of this type are used as switches of power converting units such as inverters, to which reverse conducting diodes are connected in parallel. As pointed out in Japanese Patent Laid-Open No. 61-15370, the usual power MOSFET has the reverse conducting diode built therein; but, the IGBT has no built-in diode, thus must have such a reverse conducting diode connected externally.

In view of the foregoing problems, Japanese Patent Laid-Open No. 61-15370, for example, has proposed a configuration as shown in Fig. 15. In this drawing, a portion of a p^+ layer 11 on the side of the drain (corresponding to a reverse conducting diode region 5 as shown) is replaced with an n^+ layer 11N of the opposite conduction type so that a reverse conducting diode is built in integrally. Further, an n^+ layer 25 is formed for restricting the injection of positive holes from the p^+ layer 11 on the side of the drain without affecting the on-resistance appreciably, whereby the lifetime of carriers in an n^- drain layer 12 is decreased, thereby shortening the turn-off time.

In fact, by virtue of the n^+ layer 25 disposed between the p^+ layer 11 and the n^- drain layer 12, the efficiency of injection of positive holes from the p^+ layer 11 into the n^- drain layer 12 is decreased. However, since the whole current flowing through an n^+ source layer 14 and the p^+ layer 11 is given by the sum of electrons and positive holes, the foregoing decrease in the efficiency of injection of positive holes results in a decrease in the current of positive holes which forms part of the whole current, that is, the amount of minority carrier (positive hole) accumulated in the n^- drain layer 12 decreases, and the amount of positive hole contributing to conductivity modulation in the n^- drain layer 12 also decreases; as a result, the on-resistance increases inevitably.

Another configuration as shown in Fig. 16 has also been proposed (see "Extended Abstract of the 18th Conference on Solid State Devices and Materials", Tokyo, 1986, pp. 97 - 100) which is characterized in that an n^+ region 26 is formed in a marginal surface portion of an IGBT element, and this n^+ region 26 is electrically connected to a drain electrode 22, whereby the injection of minority carrier (positive hole) into the n^- layer 12 is restricted, thereby shortening the turn-off time of the IGBT.

In this second configuration, a reverse conducting diode is virtually or parasitically built in wherein a reverse conducting current flows through the path defined by a source electrode 18, p layer 13, n^- layer 12, n^+ layer 26, external wire 34', and drain electrode 22 in that order. However, the lateral resistance of the n^- layer 12 is high especially when the IGBT is designed to exhibit a high withstand voltage. Accordingly, even if it were tried to attain the reverse conducting function by the use of the foregoing path, the resultant operating resistance is high thus, the reverse conducting diode seeming to be built in cannot function practically as required.

The present invention has been devised in view of the foregoing various problems, thus its object is to provide an insulated gate bipolar transistor (IGBT) having a reverse conducting function of low operating resistance built therein, whose turn-off time is short and whose on-resistance is low.

DISCLOSURE OF THE INVENTION

To accomplish the foregoing object, in an insulated gate bipolar transistor according to the present invention, a first semiconductor layer of a first conduction type is formed on the side of a drain, a second semiconductor layer of a second conduction type for causing conductivity modulation upon carrier injection is formed on the first semiconductor layer, a third semiconductor layer of the first conduction type is selectively formed on the surface of the second semiconductor layer, a fourth semiconductor layer of the second conduction type is selectively formed on the surface of the third semiconductor layer, a gate electrode is formed on the surface of the third semiconductor layer between the second semiconductor layer and the fourth semiconductor layer with a gate insulating film interposed between them, a source electrode is formed as to spread from the surface of the third semiconductor layer to the surface of the fourth semiconductor layer, and a drain electrode for supply of a drain current is formed on the side of the drain.

In the foregoing configuration, a fifth semiconductor layer of the second conduction type for passing therethrough a reverse conducting current

opposite in direction to the drain current is formed in a given region within the second semiconductor layer which is electrically connected to the drain electrode, and a sixth semiconductor layer of the second conduction type is formed at or in the vicinity of the interface between the first semiconductor layer and the second semiconductor layer with an impurity concentration higher than that of the second semiconductor layer into a given pattern such that a region for passage of carriers is left to decrease the electric resistance between the fifth semiconductor layer and a region of the second semiconductor layer that is spaced apart from the fifth semiconductor layer and to allow the carriers to be given and received between the first semiconductor layer and the second semiconductor layer, whereby a reverse conducting function is provided.

Specifically, by providing the fifth semiconductor layer and electrically connecting the fifth semiconductor layer to the drain electrode using a conductor, there are formed a pn junction diode composed of the second and third semiconductor layers and a transistor (referred to as a reverse transistor) whose emitter, base and collector correspond to the third, second and first semiconductor layers, respectively, whereby the reverse conducting function is provided. Further, by forming the sixth semiconductor layer of the same conduction type as of the second semiconductor layer with an impurity concentration higher than that of the second semiconductor layer, the operating resistance of the reverse conducting function is decreased by virtue of the sixth semiconductor layer. That is, the sixth semiconductor layer decreases the operating resistance of the pn junction diode and serves as the current path of the pn junction diode. Further, the current flowing through the sixth semiconductor layer becomes the base current of the reverse transistor. Accordingly, a current larger than the base current flows through the collector (the first semiconductor layer) of the reverse transistor and through the drain electrode. Therefore, the operating resistance of the reverse conducting function can be decreased and a large reverse current can be passed through it.

Further, since the second and first semiconductor layers are electrically short-circuited via the sixth and fifth semiconductor layers, excessive majority carriers accumulated in the second semiconductor layer are removed, thereby shortening the turn-off time. In this regard, since the sixth semiconductor layer is formed into a given pattern such that a region for passage of carriers is left to allow the carriers to be given and received between the first semiconductor layer and the second semiconductor layer, the passage of the carriers is not impeded. Therefore, an increase in on-resistance that would be caused if the passage of the carriers were impeded does not occur, whereby the turn-off time can be shortened.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. I is a perspective view, with portions broken away, showing a first embodiment of an insulated gate bipolar transistor (IGBT) according to the present invention;

Fig. 2 is a sectional view taken along line A-A in Fig. I;

Fig. 3 is a sectional view taken along line B-B in Fig. I;

Fig. 4 is a graph showing the electrical characteristic of the IGBT shown in Fig. I;

Fig. 5 is a diagram showing the equivalent circuit of the IGBT shown in Fig. I;

Fig. 6 is a perspective view, with portions broken away, showing a second embodiment of the IGBT according to the present invention;

Fig. 7 is a sectional view taken along line A-A in Fig. 6;

Fig. 8 is a sectional view taken along line B-B in Fig. 6;

Fig. 9 is a perspective view, with portions broken away, showing a third embodiment of the IGBT according to the present invention;

Fig. I0 is a perspective view, with portions broken away, showing a fourth embodiment of the IGBT according to the present invention;

Fig. II is a perspective view, with portions broken away, showing a fifth embodiment of the IGBT according to the present invention;

Fig. I2 is a sectional view taken along line A-A in Fig. II;

Fig. I3 is a sectional view taken along line B-B in Fig. II;

Fig. I4 is a sectional view showing a fundamental IGBT; and

Figs. I5 and I6 are sectional views showing conventional IGBT's.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiments of the present invention will now be described with reference to the drawings.

Fig. I is a perspective view showing a first embodiment of an insulated gate bipolar transistor (IGBT) according to the present invention. Figs. 2 and 3 are sectional views taken along line A-A and line B-B, respectively, in Fig. I. The process of manufacturing the IGBT will be described.

First, a semiconductor substrate is prepared having a p^+ layer II. (a first semiconductor layer), and impurities are selectively diffused into the surface of the substrate to form an n^+ layer 23 of

mesh pattern. Then, an n^- layer 12 (a second semiconductor layer) is formed by the vapor growth technique on the surface of the p^+ layer 11 (where the n^+ layer 23 is present) as to have an impurity concentration enough to realize a predetermined withstand voltage, this n^- layer 12 changing the n^+ layer 23 into the form of an embedded layer.

Then, a p layer 13 (a third semiconductor layer) and another p layer 21 are concurrently formed to a depth of 3 - 6 μm by the selective diffusion technique. This p layer 21 called a guard ring is provided for the purpose of ensuring a high withstand voltage. Further, an n^+ layer 14 (a fourth semiconductor layer) and another n^+ layer 20 are concurrently formed in the p layer 13 and in a marginal portion of the element, respectively, by the selective diffusion technique. Here, the n^+ layer 14 serves as a source, and the n^+ layer 20 serves as the cathode of a pn junction diode (referred to as a reverse conducting diode) composed of the p layer 13 and n^- layer 12, as will be described later.

In the foregoing manufacturing process, the p layer 13 and the n^+ layer 14 are formed in self alignment manner by the so-called DSA (diffusion self alignment) technique, using a gate electrode 16 as a mask which is formed on a gate oxide film 15 formed by oxidizing the surface of the n^- layer 12; as a result, there is provided a channel.

Then, an interlayer insulating film 17 is formed, and for the purpose of providing ohmic contact for the p layer 13, n^+ layer 14 and n^+ layer 20, contact openings are formed in the gate oxide film 15 and the interlayer insulating film 17, aluminum is deposited to a thickness of a few μm, and selective etching is performed to form a source electrode 18, a source terminal 31, a gate terminal 33, a reverse conducting electrode 19, and a reverse conducting terminal 32.

Then, a metallic film is deposited on the back side of the p^+ layer 11 to form a drain electrode 22, and an external conductor 34 is connected to the reverse conducting terminal 32 and the drain electrode 22, whereby an IGBT 1 is completed as shown in Figs. 1 through 3. The IGBT 1 is composed fundamentally of an element region 4, a high-voltage withstand region 3, and a marginal region 2, as shown in Figs. 1 through 3.

The operation of the foregoing configuration will be described.

The reverse characteristic or reverse conducting function of the IGBT 1 shown in Fig. 1 will be described with reference to Fig. 3. To explain the operation of the reverse conducting state, in Fig. 3, a power source V_3 and a load resistor R_L are connected between the source electrode 18 and the drain electrode 22 such that positive and negative potentials are applied to the source electrode 18 and the drain electrode 22, respectively.

In the foregoing configuration, a reverse conducting current flows through two paths: the reverse conducting diode composed of the p layer 13 and n^- layer 12; and a reverse transistor whose emitter, base and collector correspond to the p layer 13, n^- layer 12 and p^+ layer 11, respectively.

Specifically, in the reverse conducting diode, the reverse conducting current flows through the path indicated by the arrows 40 through 43 in Fig. 3, or the path defined by the positive plate of the source V_3, source electrode 18, p layer 13, n^- layer 12, n^+ embedded layer 23, n^- layer 12, n^+ layer 20, reverse conducting electrode 19 and reverse conducting terminal 32, external conductor 34, drain electrode 22, load resistor R_L, and negative plate of the source V_3 in that order.

In the foregoing path, the forward characteristic of the reverse conducting diode of the IGBT 1 is determined by the electrical characteristic of the pn junction composed of the p layer 13 and n^- layer 12, and the operating resistance determined by the path defined by the p layer 13, n^- layer 12 (arrow 41), n^+ embedded layer 23, n^- layer 12 (arrow 42), and n^+ layer 20 in that order. That is, the value of operating resistance R_1 of the reverse conducting diode is expressed by

$$R_1 = R_{10} + R_{11} + R_{12} \quad (1)$$

where R_{10} is the value of resistance encountered when the current indicated by the arrow 41 flows across the n^- layer 12, R_{11} is the value of resistance encountered when the current flows laterally across the n^+ embedded layer 23, and R_{12} is the value of resistance encountered when the current indicated by the arrow 42 flows across the n^- layer 12.

In Expression (1), the R_{10} and R_{12} are low enough. The reason is that even where the resistivity of the n^- layer 12 is as high as some tens of Ω.cm, the distance of the path indicated by the arrows 41 and 42 is as short as 100 μm at most. Further, the R_{11} is low enough. The reason is that the impurity concentration of the n^+ embedded layer 23 is made high so that its resistivity becomes less enough, and the pitch of the mesh pattern of the layer 23 is set fine enough. Accordingly, the value of operating resistance R_1 of the reverse conducting diode expressed by Expression (1) is low enough.

On the other hand, in case the n^+ embedded layer 23 is not provided, the reverse conducting current flows a long distance through the n^- layer 12 of high resistance as indicated by the arrow 44 in Fig. 3; therefore, the operating resistance of the reverse conducting diode becomes greater.

Now, in the reverse transistor, the reverse con-

ducting current flows through the path indicated by the arrow 47 in Fig. 3, or the path defined by the source electrode 18, p layer 13, n^- layer 12, p^+ layer 11, and drain electrode 22 in that order.

In the foregoing path, the forward characteristic of the reverse transistor is determined by the efficiency of injection of positive holes injected from the p layer 13 (corresponding to the emitter) into the n^- layer 12 (corresponding to the base), and the efficiency of transportation of positive holes when they move through the n^- layer 12 (corresponding to the base layer) to the p^+ layer 11 (corresponding to the collector), and the product of the injection efficiency and the transportation efficiency determines the forward current gain α of the reverse transistor. Generally, using the current gain α, the ratio of collector current I_C to base current I_B of a transistor is given by

$$\frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$$

and the value α is generally close to one (1); thus, the collector current I_C is greater than the base current I_B. In the reverse transistor composed of the p layer 13, n^- layer 12, and p^+ layer 11, the base current I_B corresponds to the current flowing through the foregoing reverse conducting diode. Accordingly, a current larger than the above flows as the collector current of the reverse transistor.

As described above, the presence of the n^+ embedded layer 23 can decrease not only the operating resistance of the reverse conducting diode but also the operating resistance of the reverse transistor; thus, the operating resistance of the reverse conducting function can be made less by the foregoing multiplicative effect.

Fig. 4 shows the electrical characteristic of the IGBT I in which the characteristic curve Y corresponds to the presence of the n^+ embedded layer 23 and the characteristic curve N to the absence. The third quadrant of the graph corresponds to the reverse conducting characteristic. As will be clear from Fig. 4, where the n^+ embedded layer 23 is present, the operating resistance is low , whereby a large current can be passed.

The forward characteristic of the IGBT I shown in Fig.1 will be described with reference to Fig. 2. To explain the operation of the forward characteristic, in Fig. 2, a power source V_2 and a load resistor R_L are connected between the drain electrode 22 and the source electrode 18, and another power source V_1 is connected between the gate electrode 16 and the source electrode 18.

In the foregoing configuration, electrons flow along the path indicated by the arrow 45, or through the n^+ layer 14, channel, n^- layer 12, mesh portion 24 of the n^+ embedded layer 23, and p^+ layer 11 in that order. On the other hand, positive holes flow along the path indicated by the arrow 46, or through the p^+ layer 11, mesh portion 24 of the n^+ embedded layer 23, n^- layer 12, and p layer 13 in that order. That is, in the IGBT I having the n^+ embedded layer 23, this embodiment makes the n^+ embedded layer 23 into the form of a mesh so that electrons and positive holes can pass through the mesh portion 24 of the n^+ embedded layer 23. Therefore, by properly setting the pitch of the mesh pattern of the n^+ embedded layer 23 such that it less influences the passage of electrons and positive holes as if the n^+ embedded layer 23 were not provided as in the prior art, it is possible to attain both high withstand voltage and low on-resistance.

Further, the IGBT I shown in Fig. 1 has the reverse conducting function built therein and its turn-off time can be shortened. The reason will be described. The equivalent circuit of the IGBT is shown in Fig. 5. Specifically, the IGBT is composed of a pnp transistor 50, an npn transistor 51, and a MOSFET 52, and a shunt resistor 54 is connected across the base-emitter to make the npn transistor 51 disable in the normal operation. Therefore, the turn-off time of the IGBT is determined by the turn-off time of the pnp transistor 50. The emitter E of the pnp transistor 50 corresponds to the p^+ layer 11 shown in Figs. 1 through 3, the base B to the n^- layer 12, and the collector C to the p layer 13.

It is known that if an adequate resistor is connected across the base-emitter of a bipolar transistor, it removes excessive charge accumulated in the base to shorten the turn-off time. That is, in Fig. 5, when a resistor 53 of low resistance is connected across the base-emitter of the pnp transistor 50, the turn-off time of the pnp transistor is shortened, thereby shortening the turn-off time of the IGBT I.

Since the base of the pnp transistor 50 corresponds to the n^- layer 12 and the emitter to the p^+ layer 11, the value of resistance R_{53} of the resistor 53 shown in Fig. 5 is expressed by

$$R_{53} = R_{11} + R_{12} \quad (2)$$

where R_{11} is the value of resistance encountered when the current flows laterally through the n^+ embedded layer 23, R_{12} is the value of resistance between the n^+ embedded layer 23 and the n^+ layer 20, and they are indentical with the R_{11} and R_{12} included in Expression (1).

As will be clear from Figs. 2 and 3, the n^+ embedded layer 23 spreads over the whole area of a junction surface 30 in the form of a mesh and is

in electrical contact with the n^- layer 12. Therefore, the R_{11} and R_{12} included in Expression (2) are less enough; thus, the R_{53} can be made low , the turn-off time of the pnp transistor 50 can be shortened, and the turn-off time of the IGBT 1 can be shortened.

As described above, in this embodiment, since the n^+ embedded layer 23 is made in the form of a mesh, the turn-off time can be shortened without degrading the efficiency of injection of positive holes from the p^+ layer 11 or increasing the on-resistance, and there is realized the configuration having the reverse conducting function built therein.

Incidentally, in this embodiment, the n^+ layer 20 can be formed concurrently with the n^+ layer 14, the n^+ embedded layer 23 of mesh pattern can be formed by adding its forming step to the manufacturing process adopted in obtaining the configuration of Fig. 14 or to a manufacturing process similar to that adopted in obtaining the usual power MOSFET, and it is not necessary to form an n^+-type region (serving as the reverse conducting diode region 5) in separated relation to a p^+-type region (serving as the element region 4) on the back side of a substrate, as opposed to the configuration of Fig. 15; thus, this embodiment can be implemented without complicating the manufacturing process. In the field of IGBT manufacture, it is known to join substrates of different conduction types together or to directly join wafers together; in this case, the n^+ embedded layer of mesh pattern may be previously formed on the surface to be joined of a substrate or wafer.

Figs. 6 through 8 show a second embodiment. Figs. 7 and 8 are sectional views taken along line A-A and line B-B, respectively, in Fig. 6. In these drawings, portions identical with those shown in Figs. 1 through 3 are designated by the same reference numerals. The configuration of Figs. 6 through 8 differs from that of Figs. 1 through 3 in that a portion of the n^+ embedded layer 23 is modified. Specifically, portions of the n^+ embedded layer 23 which are in confronting relation to the marginal region 2, high-voltage withstand region 3, source terminal 31, and reverse conducting terminal 32, namely, portions of the n^+ embedded layer 23 which are not in confronting relation to the element region 4, are uniformly spreading in contrast with the form of a mesh, thereby defining n^+ layers 233 and 231.

With the foregoing modification, a portion of the n^+ embedded layer 23 which is in confronting relation to the n^+ layer 20 becomes large in area; consequently, the value of resistance R_{12} included in Expressions (1) and (2) can be made further low so that the value of operating resistance R_1 of the reverse conducting diode of the IGBT 1 can be made further low, and the value of resistnace R_{53} across the base-emitter of the pnp transistor 50 in the equivalent circuit of Fig. 5 can be made further low , whereby the turn-off time can be shortened further.

The pattern of the n^+ embedded layer 23 may be modified to some extent. Although the first or second embodiment makes the n^+ embedded layer 23 into the form of a mesh or a lattice (defined by vertical and horizontal directions), Figs. 9 and 10 show third and fourth embodiments, respectively, which use a striped pattern (aligned in one direction). It should be noted that the pattern may be modified if the object of the n^+ embedded layer 23 is accomplished. Further, it is not necessary to form the n^+ embedded layers 233 and 231 of Fig. 6 as to confront all of the marginal region 2, high-voltage withstand region 3, source terminal 31, reverse conducting electrode 19, and reverse conducting terminal 32 of the IGBT 1, and the same effect can be obtained even when the n^+ embedded layers 233 and 231 are formed in confronting relation to some of them.

Further, the n^+ embedded layer 23 is not necessarily formed as to spread up to below the n^+ layer 20 provided that the operating resistance of the reverse conducting diode composed of the n^- layer 12 and p layer 13 can be made less enough. For example, the n^+ embedded layer 23 may be formed as to spread only up to below the high-voltage withstand region 3.

Further, the n^+ embedded layer 23 is not necessarily formed at the interface between the n^- layer 12 and the p^+ layer 11, and the same effect can be obtained even when the n^+ embedded layer 23 is formed in the n^- layer 12 in the vicinity of the interface.

A fifth embodiment of the present invention will be described with reference to Figs. 11 through 13. Fig. 11 is a perspective view, with portions broken away, showing an IGBT according to the fifth embodiment of the present invention, and Figs. 12 and 13 are sectional views taken along line A-A and line B-B, respectively, in Fig. 11. In these drawings, portions identical with those shown in Figs. 1 through 3 are designated by the same reference numerals.

The fifth embodiment shown in Figs. 11 through 13 differs from the first embodiment shown in Figs. 1 through 3 in that the n^+ embedded layer 23 is formed in embedded form in the p^+ layer 11 to a depth of ℓ from the interface (junction surface) 30 between the p^+ layer 11 and the n^- layer 12. Specifically, in the process of manufacturing an IGBT 1 similar to that described in connection with the first embodiment, impurities are selectively diffused into the surface of the p^+ layer 11 (serving as the semiconductor substrate) to form the n^+ layer 23

of mesh pattern, and after the n^- layer 12 is formed by the vapor growth technique, the wafer is subjected to heat treatment such that the n^+ embedded layer 23 is embedded in the p^+ layer 11. That is, the heat treatment for the wafer causes impurities within the p^+ layer 11 to diffuse into the n^- layer 12 so that the position of the pn junction formed between the p^+ layer 11 and the n^- layer 12 shifts towards the n^- layer 12; as a result, the n^+ embedded layer 23 is embedded in the p^+ layer 11. In this step, the distance ℓ from the junction surface 30 to the n^+ embedded layer 23 is regulated to smaller than the diffusion length of electrons by controlling the impurity concentration of a p^+ layer region 11' defined by the distance ℓ.

The operation of the foregoing configuration will be described.

The reverse characteristic or reverse conducting function of the IGBT 1 shown in Fig. 11 will be described with reference to Fig. 13. To explain the operation of the reverse conducting state, in Fig. 13, a power source V_3 and a load resistor R_L are connected between the source electrode 18 and the drain electrode 22 such that positive and negative potentials are applied to the source electrode 18 and the drain electrode 22, respectively.

In the foregoing configuration, the reverse conducting current flows through the reverse conducting diode composed of the p layer 13 and n^- layer 12, and the reverse transistor whose emitter, base and collector correspond to the p layer 13, n^- layer 12 and p^+ layer 11, respectively.

Specifically, in the reverse conducting diode, the reverse conducting current flows along the path indicated by the arrows 40 through 43 in Fig. 13, or through the path defined by the positive plate of the source V_3, source electrode 18, p layer 13, n^- layer 12, p^+ layer region 11', n^+ embedded layer 23, p^+ layer region 11', n^- layer 12, n^+ layer 20, reverse conducting electrode 19 and reverse conducting terminal 32, external conductor 34, drain electrode 22, load resistor R_L, and negative plate of the source V_3 in that order.

In the foregoing path, the forward characteristic of the reverse conducting diode of the IGBT 1 is determined by the electrical characteristic of the pn junction composed of the p layer 13 and n^- layer 12, and the operating resistance determined by the path defined by the p layer 13, n^- layer 12 (arrow 41), p^+ layer region + 11' (arrow 41), n^+ embedded layer 23, p^+ layer region 11' (arrow 42), n^- layer 12 (arrow 42), and n^+ layer 20 in that order. That is, the value of operating resistance R_f of the reverse conducting diode is expressed by

$$R_f = R_{10} + R_{11} + R_{12} + R_{13} + R_{14} \quad (3)$$

where R_{10} is the value of resistance encountered when the current indicated by the arrow 41 flows across the n^- layer 12, R_{11} is the value of resistance encountered when the current flows laterally across the n^+ embedded layer 23, R_{12} is the value of resistance encountered when the current indicated by the arrow 42 flows across the n^- layer 12, and they are identical with those included in Expression (1). Further, R_{13} is the value of resistance encountered when the current indicated by the arrow 41 flows across p^+ layer region 11', and R_{14} is the value of resistance encountered when the current indicated by the arrow 42 flows across the p^+ layer region 11'.

In Expression (3), the R_{10}, R_{11} and R_{12} are low enough as described in connection with Expression (1). In the foregoing path through which the reverse conducting current flows, since the width ℓ of the p^+ layer region 11' is set to smaller than the diffusion length of carriers, carriers can readily pass across the p^+ layer region 11'; thus, the R_{13} and R_{14} are also low enough. Accordingly, the value of operating resistance R_f of the reverse conducting diode expressed by Expression (3) becomes low enough.

On the other hand, in case the n^+ embedded layer 23 is not provided, the reverse conducting current flows a long distance across the n^- layer 12 of high resistance, as indicated by the arrow 44 in Fig. 13; thus, the operating resistance of the reverse conducting diode becomes greater.

Now, in the reverse transistor, the reverse conducting current flows along the path indicated by the arrow 47 in Fig. 13, or through the path defined by the source electrode 18, p layer 13, n^- layer 12, (p^+ layer region 11'), p^+ layer 11, and drain electrode 22 in that order. That is, as described in connection with the first embodiment, the reverse conducting current flows as the collector current of the reverse transistor which is larger than the current flowing through the foregoing reverse conducting diode.

As described above, the presence of the n^+ embedded layer 23 can decrease not only the operating resistance of the reverse conducting diode but also the operating resistance of the reverse transistor, and the operating resistance of the reverse conducting function can be made very low by the foregoing multiplicative effect. The electrical characteristic of the IGBT 1 in this embodiment is as illustrated in Fig. 4 (the characteristic curve Y) or similar to that of the first embodiment.

The forward characteristic of the IGBT 1 shown in Fig. 11 will be described with reference to Fig. 12. To explain the operation of the forward characteristic, in Fig. 12, a power source V_2 and a load resistor R_L are connected between the drain electrode 22 and the source electrode 18, and another power source V_1 is connected between the gate electrode 16 and the source electrode 18.

In the foregoing configuration, electrons flow along the path indicated by the arrow 45, or through the path defined by the n^+ layer 14, channel, n^- layer 12, (p^+ layer region 11', mesh portion 24 of the n^+ embedded layer 23), and p^+ layer 11 in that order; on the other hand, positive holes flow along the path indicated by the arrow 46, or through the path defined by the p^+ layer 11, (mesh portion 24 of the n^+ embedded layer 23, p^+ layer region 11'), n^- layer 12, and p layer 13 in that order. That is, in this embodiment, although the n^+ embedded layer 23 is formed, electrons and positive holes can pass through the mesh portion 24 of the n^+ embedded layer 23, carriers can be given and received through the whole surface of the junction surface 30 between the p^+ layer 11 (p^+ layer region 11') and the n^- layer 12, and the n^+ embedded layer 23 does not impede the flowing of electrons and positive holes, whereby a high withstand voltage and a low on-resistance can be attained, as in the prior art with no inclusion of the n^+ embedded layer 23.

Further, the IGBT 1 shown in Fig. 11 has the reverse conducting function built therein and can shorten the turn-off time. The reason will be described. As described in connection with the first embodiment, the equivalent circuit of the IGBT 1 is as shown in Fig. 5, and the turn-off time of the IGBT is determined by the turn-off time of the pnp transistor 50. The emitter E of the pnp transistor 50 corresponds to the p^+ layer 11 shown in Figs. 11 through 13, the base B to the n^- layer 12, and the collector C to the p layer 13. In this embodiment, the value of resistance R_{53} of an adequate resistor 53 being connected between the base B and the emitter E in order to remove excessive charge accumulated in the base B to thereby shorten the turn-off time is expressed by

$$R_{53} = R_{11} + R_{12} + R_{13} + R_{14} \quad (4)$$

where R_{11} is the value of resistance encountered when the current flows laterally across the n^+ embedded layer 23, R_{12} is the value of resistance encountered when the current flows across the n^- layer 12, R_{13} and R_{14} are resistances encountered when the current flows across the p^+ layer region 11', and they are identical with the R_{11} to R_{14} included in Expression (3).

As will be clear from Figs. 12 and 13, the n^+ embedded layer 23 spreads enough in the form of a mesh in parallel to the junction surface 30. Since the width ℓ of the p^+ layer region 11' is set to smaller than the diffusion length of carriers, carriers can readily go across the p^+ layer region 11'; thus, the value of resistance R_{13} and R_{14} are low enough. Also, the R_{11} and R_{12} included in Expression (4) are low enough as described above. Accordingly, the R_{53} can be made low , the turn-off time of the pnp transistor 50 can be shortened, and the turn-off time of the IGBT 1 can be shortened.

As described above, in this embodiment, the n^+ embedded layer 23 is made in the form of a mesh and formed at a position spaced the distance ℓ (smaller than the diffusion length of carriers) from the junction surface 30 towards the p^+ layer 11; thus, the area of the junction surface 30 between the p^+ layer 11 and the n^- layer 12 little decreases. Accordingly, the turn-off time can be shortened without degrading the efficiency of injection of positive holes from the p^+ layer 11 or increasing the on-resistance, and there is realized the configuration having the reverse conducting function built therein.

In the fifth embodiment, the turn-off time can be controlled by changing the distance ℓ.

The process of forming the n^+ embedded layer 23 in the p^+ layer 11 at the position spaced the distance ℓ from the junction surface 30 can be carried out by the use of the foregoing heat treatment, by forming the p^+ layer by the vapor growth technique after forming, the n^+ embedded layer 23 by the diffusion technique, by the use of the direct wafer joining technique, etc.

Further, in the fifth embodiment wherein the n^+ embedded layer 23 is formed in the p^+ layer 11, the pattern of the n^+ embedded layer 23 may be modified, as in the foregoing second, third and fourth embodiments, if the object of the n^+ embedded layer 23 is accomplished.

In all the embodiments, the high-voltage withstand region 3 is not necessarily formed depending on the service condition of the IGBT.

Although all the embodiments use the p type and n type as the first conduction type and second conduction type, respectively, the present invention is valid even when the opposite conduction type is used.

INDUSTRIAL APPLICABILITY

As described above, the insulated gate bipolar transistor according to the present invention is usable as a power element for which high withstand voltage and low on-resistance are required, and when used as a power switching element of power converting units such as inverters for driving motors in PWM (pulse width modulation) control mode, it is very effective because its built-in reverse conducting function can circulate the motor current.

Claims

1. An insulated gate bipolar transistor with a reverse conducting function comprising :

a first semiconductor layer of a first conduction type;

a second semiconductor layer of a second conduction type which is in contact with the first semiconductor layer;

a third semiconductor layer of the first conduction type which is formed in the second semiconductor layer such that its junction portion terminates at the surface of the second semiconductor layer;

a fourth semiconductor layer of the second conduction type which is formed in the third semiconductor layer such that its junction portion terminates at the surface of the third semiconductor layer;

a gate electrode formed on at least a channel region defined in the surface of the third semiconductor layer between the second semiconductor layer and the fourth semiconductor layer with a gate insulating film interposed between them;

a source electrode whose contact portion is in contact with both the third semiconductor layer and the fourth semiconductor layer;

a drain electrode for supply of a drain current through the first semiconductor layer;

a fifth semiconductor layer of the second conduction type which is electrically connected to the drain electrode and formed in a given region within the second semiconductor layer as to pass therethrough a reverse conducting current opposite in direction to the drain current; and

a sixth semiconductor layer of the second conduction type which is formed at or in the vicinity of the interface between the first semiconductor layer and the second semiconductor layer with an impurity concentration higher than that of the second semiconductor layer into a given pattern such that a region for passage of carriers is left to decrease the electric resistance between the fifth semiconductor layer and a region of the second semiconductor layer that is spaced apart from the fifth semiconductor layer and to allow the carriers to be given and received between the first semiconductor layer and the second semiconductor layer.

2. An insulated gate bipolar transistor according to claim 1, wherein the sixth semiconductor layer has a contact surface in contact with the second semiconductor layer and is formed into a given pattern such that a region for passage of carriers is set by leaving a contact surface between the first semiconductor layer and the second semiconductor layer which allows the carriers to be given and received between the first semiconductor layer and the second semiconductor layer.

3. An insulated gate bipolar transistor according to claim 1, wherein the sixth semiconductor layer is formed in the first semiconductor layer in the vicinity of the interface between the first semiconductor layer and the second semiconductor layer at a position spaced apart from the interface between the first semiconductor layer and the second semiconductor layer by a distance smaller than the diffusion length of minority carriers in the first semiconductor layer into a given pattern such that a region for passage of majority carriers through the first semiconductor layer is left to allow the carriers to be given and received between the first semiconductor layer and the second semiconductor layer.

4. An insulated gate bipolar transistor according to claim 1, wherein the given pattern is a mesh pattern or striped pattern in at least a region confronting the third semiconductor layer.

5. An insulated gate bipolar transistor according to claim 2, wherein the given pattern is a mesh pattern or striped pattern in at least a region confronting the third semiconductor layer.

6. An insulated gate bipolar transistor according to claim 3, wherein the given pattern is a mesh pattern or striped pattern in at least a region confronting the third semiconductor layer.

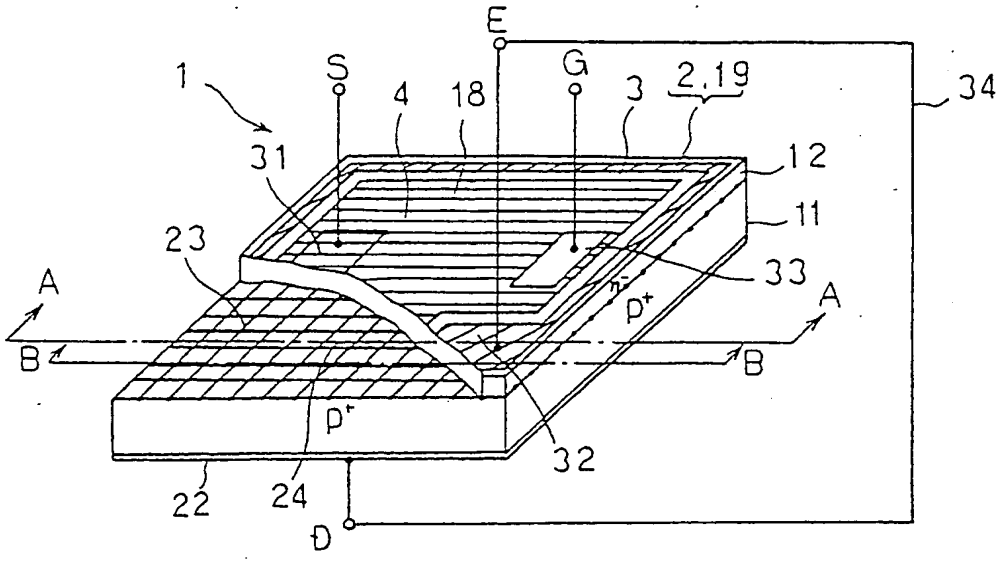
7. An insulated gate bipolar transistor according to claim 1, wherein the fifth semiconductor layer is formed in a marginal surface portion of the second semiconductor layer and electrically connected via a conductor to the drain electrode.

8. An insulated gate bipolar transistor according to claim 7, wherein the sixth semiconductor layer is formed at or in the vicinity of the interface between the second semiconductor layer and the first semiconductor layer as to spread up to a region confronting the fifth semiconductor layer that is formed in the marginal surface portion of the second semiconductor layer.

9. An insulated gate bipolar transistor according to claim 8, wherein the region confronting the fifth semiconductor layer is formed such that it is thoroughly covered with the sixth semiconductor layer at or in the vicinity of the interface between the first semiconductor layer and the

second semiconductor layer.

FIG.1


E
S
G
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3
2,19
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11
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A
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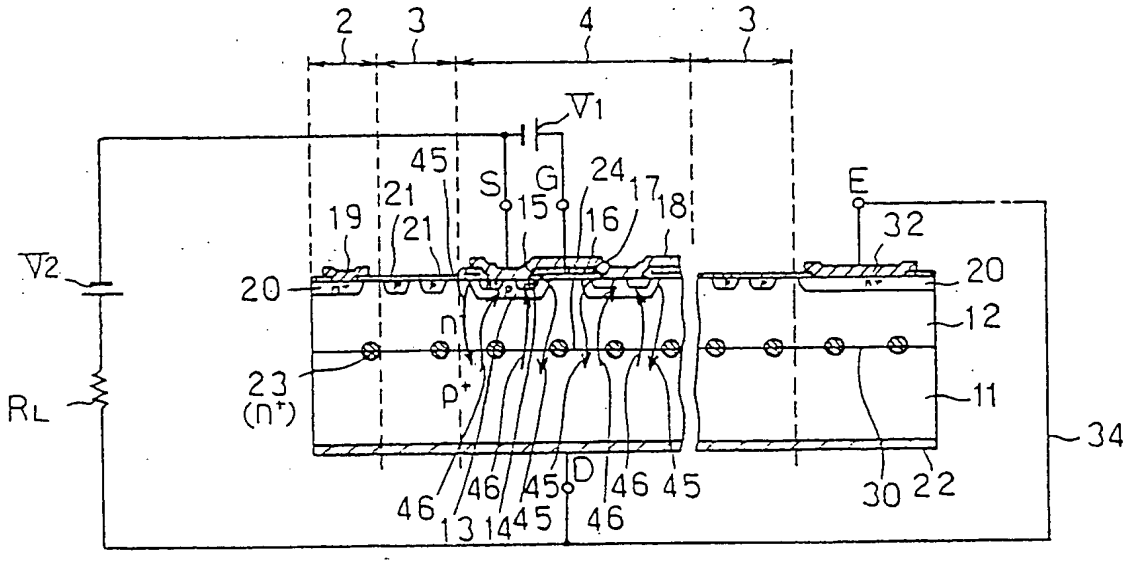
B
B
n⁻
p⁺
p⁺
32
22
24
D

FIG.2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4
3
V1
45
S
G
24
17
E
21
19
21
15
16
18
32
V2
20
20
n⁻
12
23
(n⁺)
p⁺
11
RL
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D
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46 45
30
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FIG.3

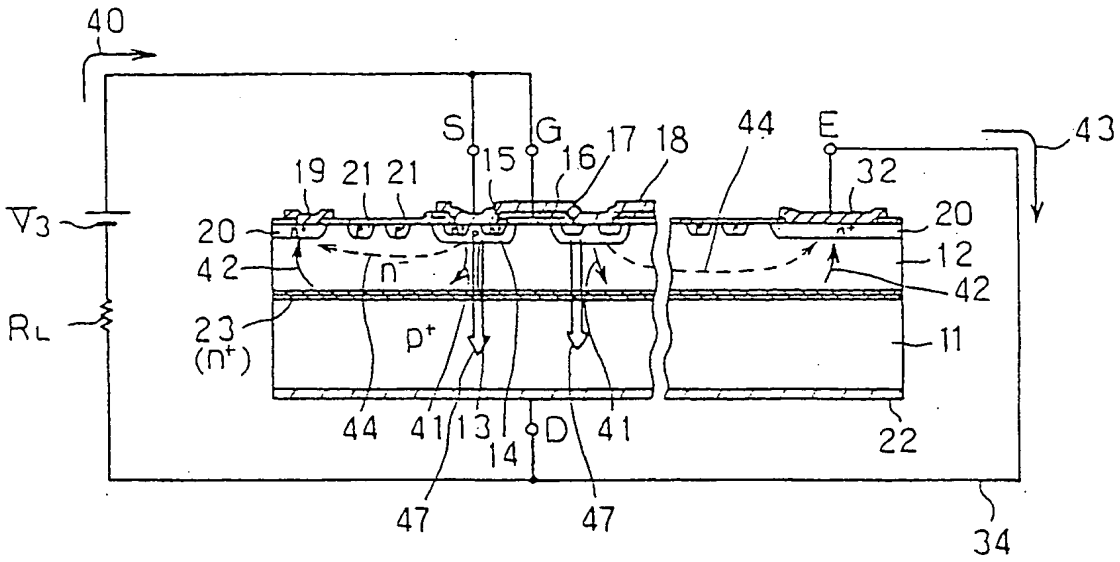


FIG.4

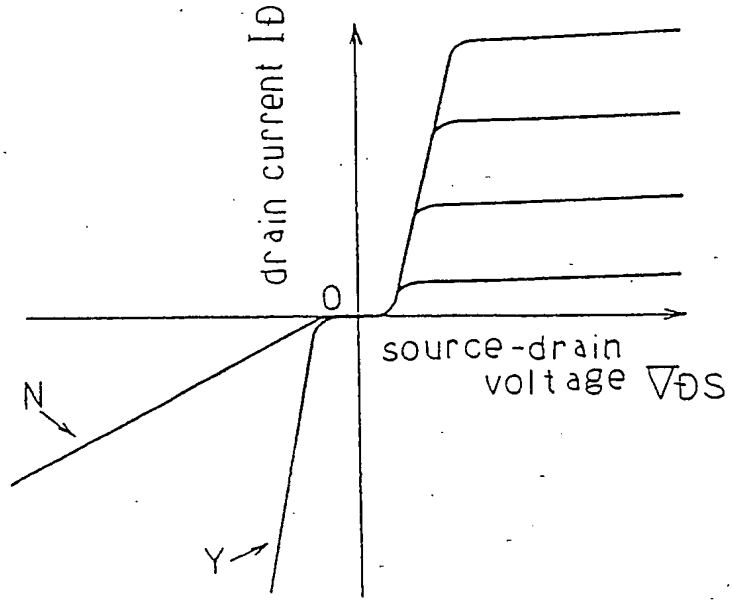


FIG.5

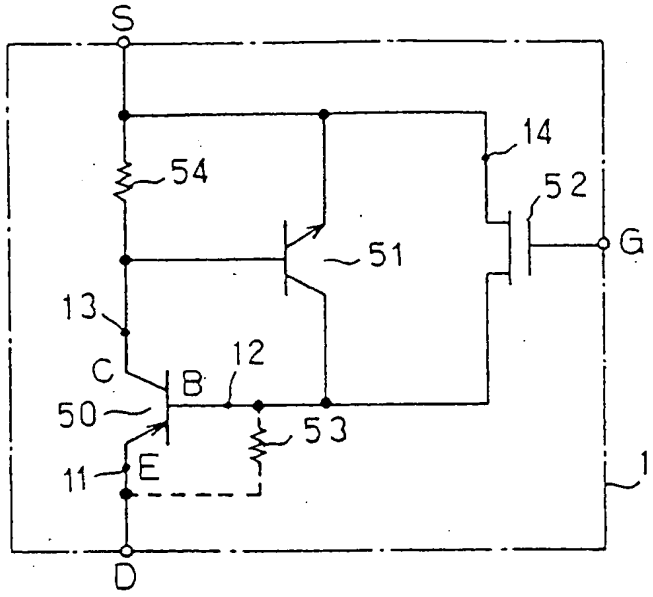


FIG.6

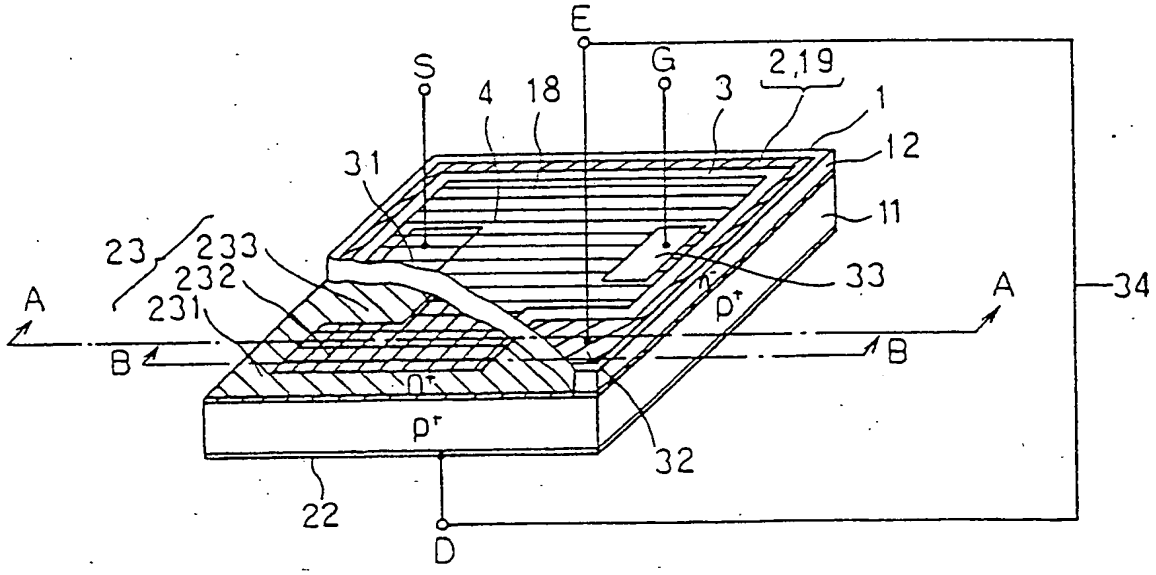
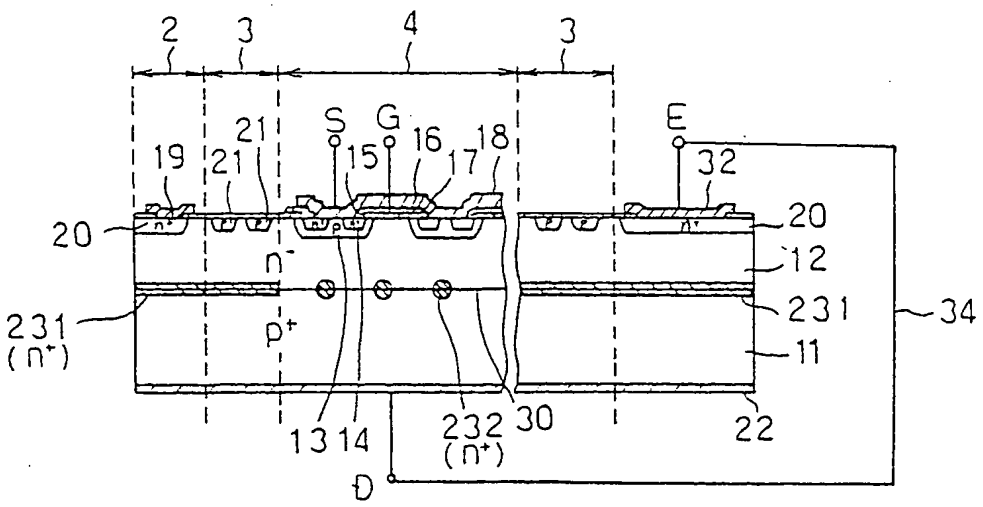


FIG.7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21
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16
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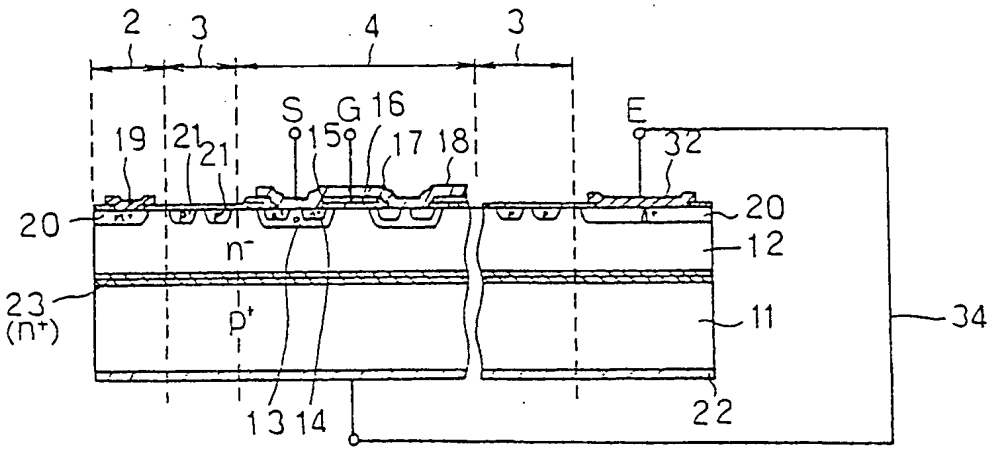
18
32
20
20
n⁻
12
231
(n⁺)
p⁺
231
34
11
13
14
232
(n⁺)
30
22
D

FIG.8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n⁻
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p⁺
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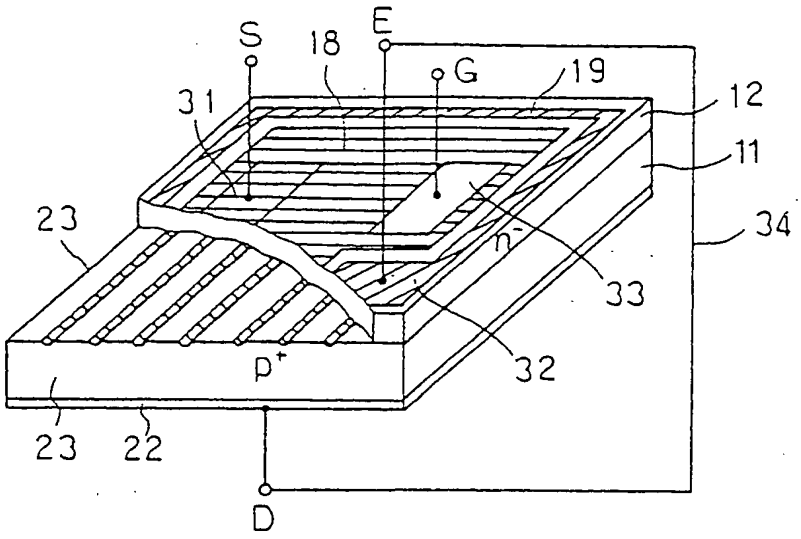
FIG.9


S
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n⁻
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p⁺
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D

FIG.10

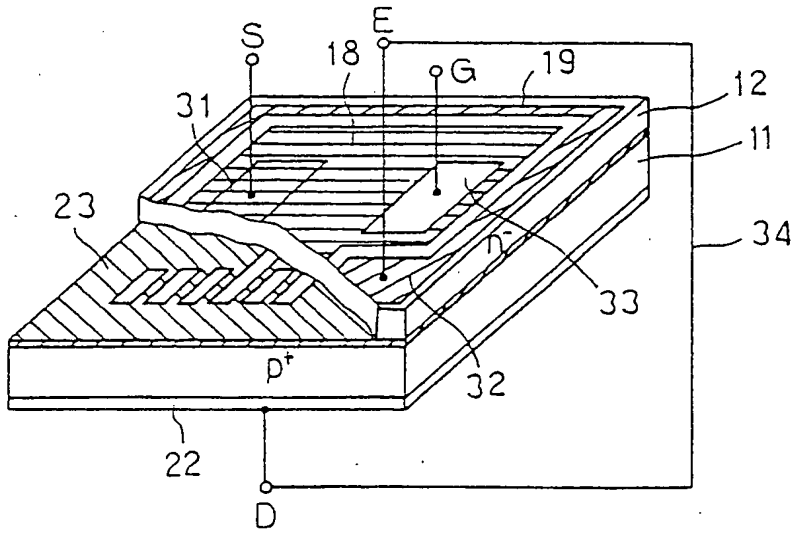
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FIG.11

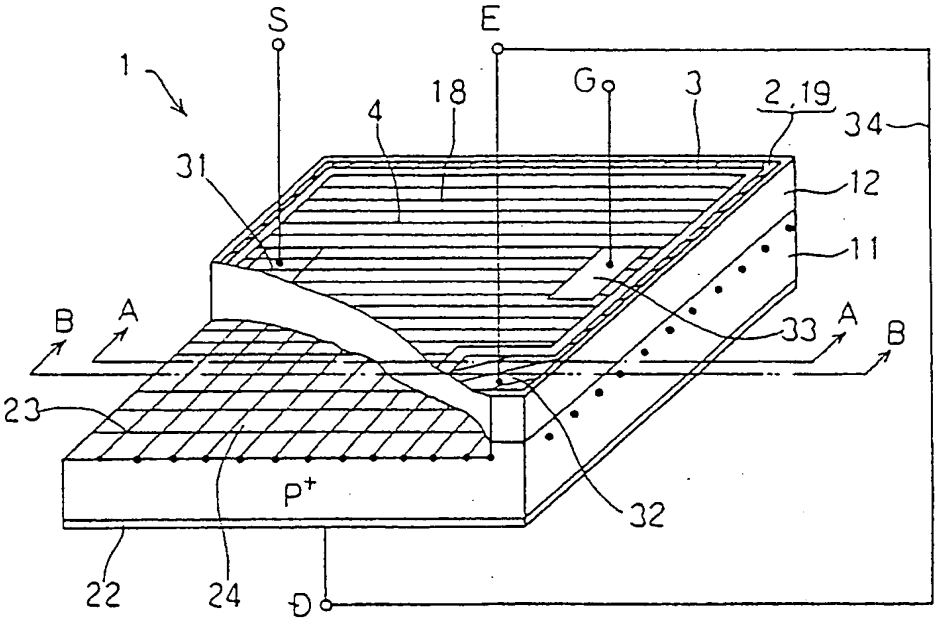


FIG.12

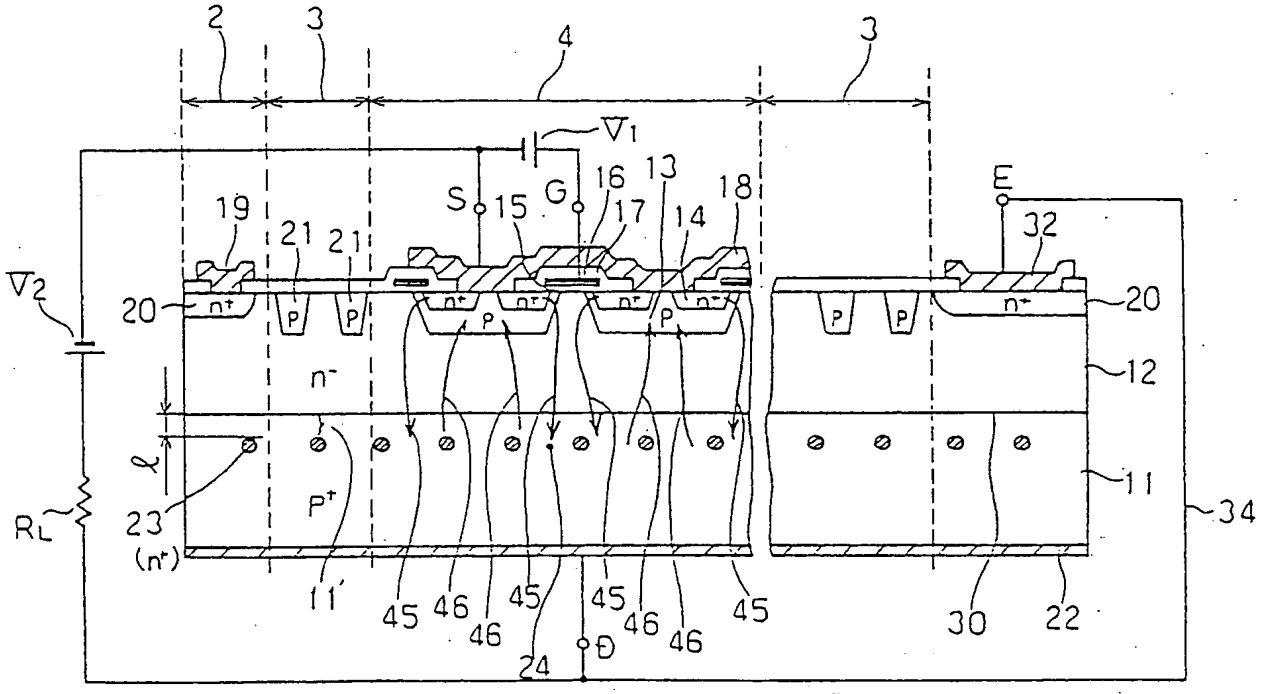
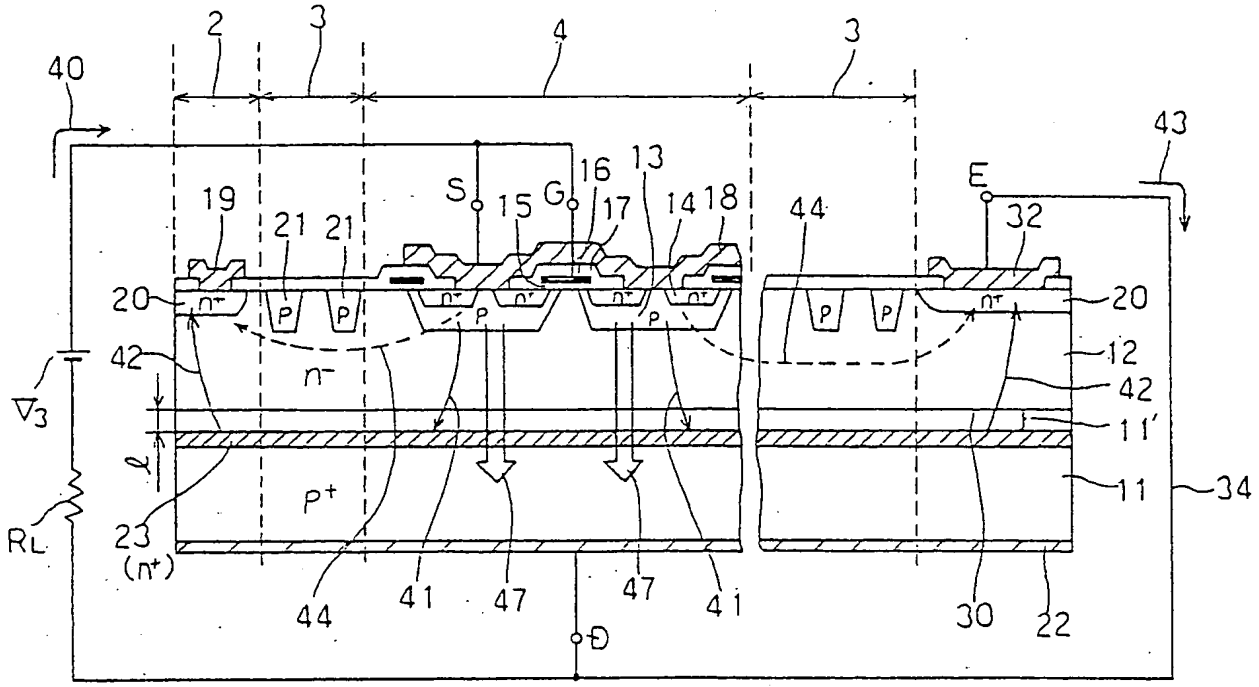


FIG.13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11'
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V_3
ℓ
R_L
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(n^+)
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47
47
41
30
22
D

FIG 14

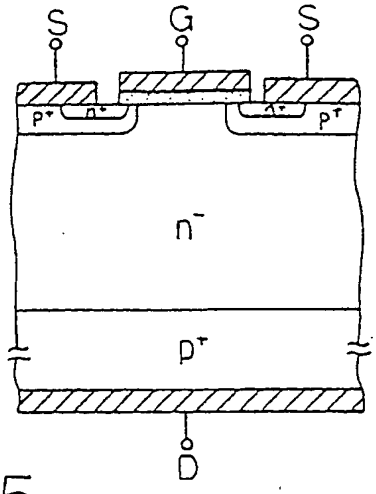


FIG.15

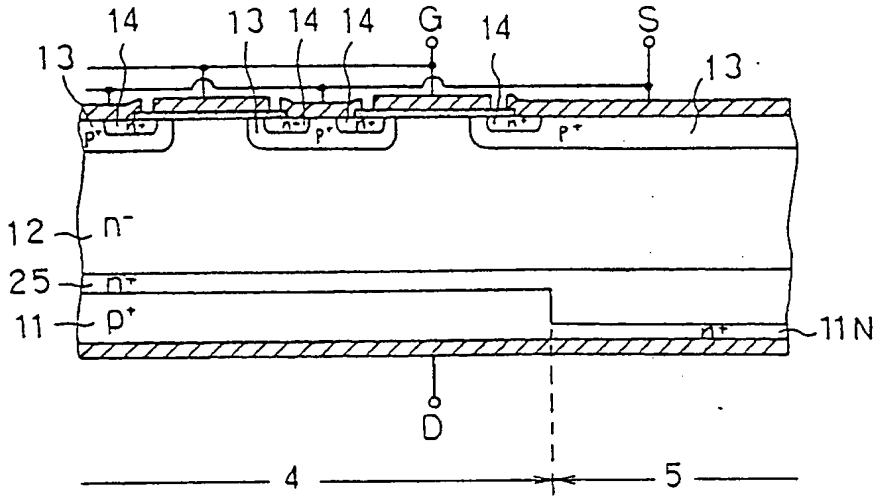
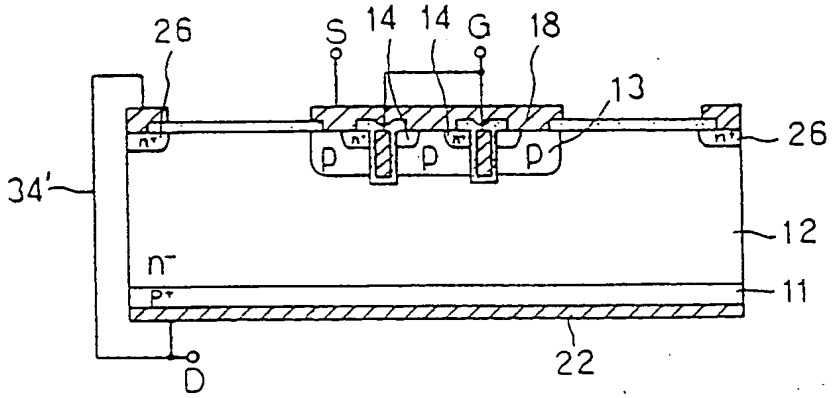


FIG.16



INTERNATIONAL SEARCH REPORT

International Application No PCT/JP90/01091

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl[5] H01L29/784

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC	H01L29/78, H01L29/68

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

Jitsuyo Shinan Koho	1965 - 1990
Kokai Jitsuyo Shinan Koho	1971 - 1990

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [9]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	JP, A, 1-109769 (Mitsubishi Electric Corp.), 26 April 1989 (26. 04. 89), (Family: none)	1 - 9
Y	JP, A, 63-150970 (Fuji Electric Co. Ltd.), 23 June 1988 (23. 06. 88), (Family: none)	1 - 9
Y	JP, A, 63-18675 (Toshiba Corp.), 26 January 1988 (26. 01. 88), (Family: none)	1 - 9

* Special categories of cited documents: [10]

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
November 9, 1990 (09. 11. 90)	November 26, 1990 (26. 11. 90)
International Searching Authority	**Signature of Authorized Officer**
Japanese Patent Office	